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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,266	03/31/2004	Douglas Holberg	CYGL-26,655	9833
25883	7590	07/26/2005		
HOWISON & ARNOTT, L.L.P P.O. BOX 741715 DALLAS, TX 75374-1715			EXAMINER NGUYEN, HIEP	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

14.13

Office Action Summary	Application No. 10/816,266	Applicant(s) HOLBERG ET AL.	
	Examiner Hiep Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 03-29-05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION***Drawings***

The drawings are objected to under 37 CFR 1.83(a) because they fail to show the “gain controller” in claim 9, line 13. The drawings are not legible. The Applicant is requested to submit a formal drawing.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation “a first rate” on line 4 is indefinite because it is not clear what it is meant by. The sampling of the input is done by clock Ø1. It is not clear if the “a first rate” is the time clock Ø1 is high. The recitation “dumping charge from the input sampling capacitor to the non inverting input of the amplifier at a second time and at the first rate” is indefinite because it is misdescriptive. Figure 2 of the present application shows that signals Ø1 and Ø2 have different duty cycles. Thus, at a second time, the charge of the sampling capacitor is dumped to the non-inverting input at the **second rate** corresponding to duty cycle of clock Ø2, not the first rate as recited.

The recitation “sampling a reference voltage onto a feedback sampling capacitor at substantially the first rate” is indefinite because it is misdescriptive. The feedback sampling capacitor (C2) samples the reference voltage when switch (134) closes with a “rate” (Ø1/D) and switch (152) closes at rate Ø1 (first rate). Thus, with the combination of these two rates, sampling a reference voltage onto a feedback sampling capacitor is not done at substantially the first rate (Ø1). Clear explanation is required.

Regarding claim 2, the recitation “the first rate” is indefinite because of the same reason raised above. The recitation “generating a second clock with a second stream of periodic pulses and shifted **in phase from** the first clock and **synchronous therewith**” is indefinite

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because it is misdescriptive. Figure 2 of the present application shows that the first and second clocks Ø1 and Ø2 are **not in phase** and they are **not in synchronism**. In fact, clock Ø1 and Ø2 are 180 degrees out of phase. Clear explanation is required.

Regarding claim 9, the recitations “a first rate” on line 5, “a second time”, “the first rate” on line 8, “the first rate” on line 10, “a second rate”, “the first rate” on line 12, “the second rate” and the first rate” on line 16 have the same 112,2nd problem raised above. The recitation “an input sampling... at substantially at the first rate” on lines 5-8 is indefinite because it is misdescriptive. Sampling the input voltage and dumping charge are controlled by different clock signals Ø1 and Ø2 having different duty cycles, thus they are not at the same rate (a first rate). The recitation “ sampling the input voltage onto the feedback sampling capacitor” on line 7 is indefinite because it is misdescriptive. Figure 1 of the present application shows that the input voltage (Vin) is sampled onto the input sampling capacitor (C1). The recitation “ a gain controller” on line 13 is indefinite because it is not clear what it is. This “gain controller” is not seen in the drawing and it is not disclosed in the specification. It is not clear how the gain controller can control the “amount of time” and what the recitation “varying the second rate relative to the first rate changes the gain of delta-signal converter” is meant by.

Regarding claim 10, the recitations “the first rate” and “generating a second stream of periodic pulses and **shifted in phase** from said **first clock** and **synchronous therewith**” are indefinite because it is not clear what the recitations “the first rate”, “shift in phase” and “synchronous therewith” are meant by. Figure 2 of the present application shows no clocks which are **in phase and in synchronism**. Clear explanation is required.

Claims 3-8 and 11-16 are indefinite because of the technical deficiencies of claims 1 and 6.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin (USP. 6,107,871).

Regarding claim 1, figure 6 or 7 of Shin shows a method for driving the input of an integrator in a delta-sigma converter having an amplifier with a non-inverting input, an output and a positive input connected to a reference voltage and an integration capacitor connected between the non-inverting input and the output, comprising the steps of:

sampling an input voltage (V_{in}) at a first rate (ϕ_1) onto an input sampling capacitor ($C/4$);

dumping charge from the input sampling capacitor ($C/4$) to the non-inverting input of the amplifier at a second time (ϕ_2) and at a second rate;

sampling a reference voltage (V_{in}) onto a input sampling capacitor ($C/4$) at substantially the "first rate" (ϕ_1);

dumping charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier at a second rate (ϕ_2) different than the first rate; and

controlling the amount of time that charge is dumped from the feedback sampling capacitor to be substantially equal to the amount of time that charge is being dumped from the input sampling capacitor (note that the dumping of the charges onto the negative feedback of the amplifier is performed with the same clock signal (ϕ_2);

wherein varying the second rate relative to the first rate changes the gain of delta-sigma converter.

Regarding claims 2 and 3, the steps of sampling an input voltage at the first rate onto (ϕ_1) an input sampling capacitor ($C/4$) and dumping charge from the input sampling capacitor to the non-inverting input of the amplifier comprise:

generating a first clock (ϕ_1) with a first stream of periodic pulses at the first rate;

generating a second clock (ϕ_2) with a second stream of periodic pulses and "shifted in phase from the first clock and synchronous" therewith;

sampling the input voltage onto the input sampling capacitor ($C/4$) during the time that the first stream of pulses (ϕ_1) are high; and

dumping charge from the input sampling capacitor ($C/4$) to the non-inverting input of the amplifier during the time that the second stream of pulses (ϕ_2) are high. Pulses (ϕ_1) and (ϕ_2) are non overlapping

Regarding claim 4, the step of sampling the input voltage on the input sampling capacitor comprises the steps of connecting one plate of the input sampling capacitor ($C/4$) to the input voltage (V_{in}) and the other plate of the input sampling capacitor to ground during the time that the first stream of pulses (ϕ_1) are high; and

the step of dumping charge from the input sampling capacitor to the non-inverting input of the amplifier comprises the steps of connecting the one plate of the input sampling capacitor ($C/4$) to ground and the other plate of the input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (ϕ_2) are high.

Regarding claim 5, the steps of sampling the reference voltage onto the feedback sampling capacitor and dumping charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier comprises the steps of:

sampling the reference voltage (V_{in}) onto the feedback sampling capacitor ($C/4$) during the time that the first stream of pulses (ϕ_1) are high; and

dumping charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (ϕ_2) are high and at a different rate than the step of sampling the reference voltage onto the feedback sampling capacitor.

Regarding claim 6, the step of sampling the reference voltage on the feedback sampling capacitor comprises the steps of connecting one plate of the feedback sampling capacitor ($C/4$) to the reference voltage (V_{in}) and the other plate of the feedback sampling capacitor to ground during the time that the first stream of pulses (ϕ_1) are high; and the step of dumping charge from the feedback sampling capacitor ($C/4$) to the non-inverting input of the amplifier comprises the steps of connecting the one plate of the feedback sampling capacitor to ground and the other plate of the feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (ϕ_2) are

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high and at a different rate than the step of sampling the reference voltage onto a feedback sampling capacitor. Note that signals ($\phi 1$) and ($\phi 2$) have different duty cycles.

Regarding claim 7, the step of dumping charge stored on the feedback sampling capacitor ($C/4$) to the non-inverting input of the amplifier occurs during the time that select ones of the pulses in the second stream of pulses are high, and the number of the pulses in the second stream of pulses during which the step of dumping charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier is less than all of the pulses in the second stream of pulses.

Regarding claim 8, the step of generating a control signal in a control circuit, not shown that generates and regulating signals ($\phi 1$) and ($\phi 2$), that selects the ones of the pulses in the second stream of pulses during which charge stored on the feedback sampling capacitor is dumped to the non-inverting input of the amplifier.

Regarding claim 9, figure 6 of Shin shows a gain control circuitry for driving the input of an integrator in a delta-sigma converter having an amplifier with a non-inverting input, an output and a positive input connected to a reference voltage and an integration capacitor connected between the non-inverting input and the output comprising:

- an input sampling circuit (SW1, SW4) for sampling an input voltage at a first rate ($\phi 1$) onto an input sampling capacitor ($C/4$);

- a first dump circuit (SW2, SW3) for dumping charge from said input sampling capacitor to the non-inverting input of the amplifier at a second time and at the first rate;

- a feedback sampling circuit (SW13, SW16) for sampling a reference voltage (V_{in}) onto a feedback sampling capacitor at substantially the first rate ($\phi 1$);

- a second dump circuit (SW14, SW15) for dumping charge stored on said feedback sampling capacitor ($C/4$) to the non-inverting input of the amplifier at a second rate ($\phi 2$) different than the first rate; and

- a gain controller, not shown, for controlling the amount of time (the duty cycle of $\phi 2$) that charge is dumped from said feedback sampling capacitor ($C/4$) to be substantially equal to the amount of time ($\phi 2$) that charge is being dumped from said input sampling capacitor;

wherein varying the second rate relative to the first rate changes the gain of delta-sigma converter.

Regarding claim 10, the first dump circuit comprises:

a first clock for generating a first stream of periodic pulses (ϕ_1) at the first rate;

a second clock for generating a second stream of periodic pulses (ϕ_2) and

“shifted in phase from said first clock and synchronous therewith”;

first switching circuitry (SW1, SW4) for sampling the input voltage onto the non-inverting input of the amplifier during the time that the first stream of pulses (ϕ_1) are high; and

second switching circuitry (SW2, SW3) for dumping charge from said input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (ϕ_2) are high.

Regarding claim 11, the first stream of periodic pulses and said second stream of periodic pulses are non overlapping (Fig. 8).

Regarding claim 12, the first switching circuitry includes

a first switch (SW1) for connecting one plate of said input sampling capacitor to the input voltage; and

a second switch (SW4) for connecting the other plate of said input sampling capacitor to ground during the time that the first stream of pulses are high; and

said second switching circuitry includes:

a third switch (SW3) for connecting the one plate of said input sampling capacitor to ground; and

a fourth switch (SW2) for connecting the other plate of said input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (ϕ_2) is high.

Regarding claim 13, the second sampling circuit and said second dump circuit comprise:

third switching circuitry for sampling said reference voltage (V_{ref}) onto the non-inverting input of the amplifier during the time that the first stream of pulses (ϕ_1) are high; and

second switching circuitry for dumping charge from said feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses ($\emptyset 2$) are high and at a different rate than the rate at which the reference voltage is sampled onto said feedback sampling capacitor.

Regarding claim 14, the third switching circuitry includes:

a fifth switch (SW13) for connecting one plate of said feedback sampling capacitor to the reference voltage (VINN), and

a sixth switch (SW16) for connecting the other plate of said feedback sampling capacitor to ground during the time that the first stream of pulses are high; and said fourth switching circuitry includes:

a seventh switch (SW15) for connecting the one plate of said feedback sampling capacitor to ground, and

an eighth switch (SW14) for connecting the other plate of said feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses ($\emptyset 2$) are high and at a different rate than the rate at which the reference voltage is sampled onto said feedback sampling capacitor.

Regarding claim 15, the dumping of charge stored on said feedback sampling capacitor to the non-inverting input of the amplifier occurs during the time that select ones of the pulses in the second stream of pulses ($\emptyset 2$), and the number of the pulses in the second stream of pulses during which dumping of charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier is less than all of the pulses in the second stream of pulses (Fig. 8).

Regarding claim 16, the control signal (not shown) that selects the ones of the pulses in the second stream of pulses ($\emptyset 2$) during which charge stored on the feedback sampling capacitor is dumped to the non-inverting input of the amplifier.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

07-20-05



MY-TRANG NUTON
PRIMARY EXAMINER

5/21/05